L10: Entry 45 of 67 File: USPT Feb 6, 2001

DOCUMENT-IDENTIFIER: US 6185704 B1
TITLE: System signaling schemes for processor and memory module

Detailed Description Text (87):
Option 1: The shared SDRAM is only eligible for DSP access when all pages are known to be closed (after a PALL command). This will ensure that there are no page conflicts between the host and the DSP. After the point of memory eligibility, the host controller must drive /Sn low and monitor the wait signal before issuing any new commands. The ACTV command can then be asserted in the cycle following the cycle where /MWAITn is sampled as high. This option would work most efficiently if the host controller closed all pages at the end of every memory access. This option treats the SDRAM much like a (single bank) standard DRAM. See FIG. 16.

Detailed Description Text (107):
Option 1: The shared SDRAM is only eligible for DSP access when all pages are known to be closed (after a PALL command). This will ensure that there are no page conflicts between the host and the DSP. After the point of memory eligibility, the host controller must drive /Sn low and monitor the wait signal before issuing any new commands. The ACTV command can then be asserted in the cycle following the cycle where /MWAIT is sampled as high. This option would work most efficiently if the host controller closed all pages at the end of every memory access. This option treats the SDRAM much like a (single bank) standard DRAM. See FIG. 21.

Detailed Description Text (127):
Option 1: The shared SDRAM is only eligible for DSP access when all pages are known to be closed (after a PALL command). This will ensure that there are no page conflicts between the host and the DSP. After the point of memory eligibility, the host controller must drive /Sn low and monitor the wait signal before issuing any new commands. The ACTV command can then be asserted in the cycle following the cycle where /MnWAIT/IRQ is sampled as high. This option would work most efficiently if the host controller closed all pages at the end of every memory access. This option treats the SDRAM much like a (single bank) standard DRAM. See FIG. 26.

Detailed Description Text (147):
For this option, the shared SDRAM shall only be eligible for DSP access when all pages are known to be closed (after a PALL command). This greatly simplifies the memory controller design, making it easy for the controller to determine where the region of eligibility begins. This will ensure that there are no page conflicts between the host and the DSP. This option would work most efficiently if the host controller closed all pages at the end of every memory access. This option treats the SDRAM much like a (single bank) standard DRAM.

Detailed Description Text (164):
Option 1: The shared SDRAM is only eligible for DSP access when all pages are known to be closed (after a PALL command). This will ensure that there are no page conflicts between the host and the DSP. After the point of memory eligibility, the host controller must drive /Sn low and monitor the wait signal before issuing any new commands. The ACTV command can then be asserted in the cycle following the cycle where /MWAIT/IRQ is sampled as high. This option would work most efficiently if the host controller closed all pages at the end of every memory access. This option treats the SDRAM much like a (single bank) standard DRAM. See FIG. 31.